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NAVSPACECOM Space Surveillance Sensor System Digital Signal Processing Receiver

Volume 4—Hardware Interfaces

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13. ABSTRACT (*Maximum 200 words*)

This is a system description of the Naval Space Command (NAVSPACECOM) Space Surveillance Sensor System Digital Signal Processing Receiver (DSPR). Formerly known as NAVSPASUR, the Space Surveillance system began as an advanced research project in June 1958, was commissioned as a operational Naval command in February 1961, and is operated by NAVSPACECOM's Space Surveillance Processing Center in Dahlgren, Virginia. The DSPR is a real-time radar data acquisition and analysis system. Its function is to detect, with no prior information, all space objects whose orbits cross the continental United States and to compute their subsequent orbits. It provides vital satellite information in support of national defense mission objectives of space intelligence, satellite attack warning, satellite intercept support, and space mission support. This system description was prepared as part of a modernization program that has replaced DSPR hardware for which parts are no longer available.

Volume 3 describes the operating system functions required by the applications software. Volume 4 describes the hardware interfaces between the major subsystems of the DSPR and identifies critical timing paths and interrupts between subsystems. Previously published, Volume 1 (NRL/FR/8154--93-9577) presents an overview of the hardware and software of the DSPR system, and Volume 2 (NRL/FR/8154--93-9578) discusses the function and capabilities of individual software and hardware components of each subsystem.

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Volume 4—Hardware Interfaces

1. INTRODUCTION

This is Volume 4 of a four-volume system description of the Naval Space Command (NAVSPACECOM) Space Surveillance Sensor System Digital Signal Processing Receiver (DSPR) hardware and software. The hardware was developed by the Naval Research Laboratory (NRL) for the NAVSPACECOM Space Surveillance System (formerly NAVSPASUR). The software was designed by NRL and developed jointly by Digital Equipment Corporation (DEC) and NRL. The modernized software described in this volume was designed and developed by NRL.

The NAVSPACECOM Space Surveillance system began as an advanced research project in June 1958. In October 1960, the project was transferred from the Advanced Research Projects Agency (ARPA) to the Navy, and was subsequently commissioned as an operational Naval command in February 1961. Since then, it has been operated by the NAVSPACECOM Space Surveillance Processing Center in Dahlgren, Virginia. The Processing Center is responsible to the Chief of Naval Operations for support to the operating forces of the United States Navy, and is under the operational control of the U.S. Space Command, Colorado Springs, Colorado, for those space object data collection functions that are part of the National Space Detection and Tracking System (SPADATS).

1.1 Purpose and Scope

This volume describes the hardware interfaces between the major subsystems of the DSPR and identifies the critical timing paths and interrupts between different subsystems in terms of their current functionality. Volume 1 presents a hardware and software overview of the DSPR system. Volume 2 describes the function and capabilities of individual software and hardware components of the system. Volume 3 describes the operating system functions that are required by the applications software.

The documentation supports a project that has replaced DSPR hardware for which parts are no longer available. Hardware replaced includes the DEC PDP-11/60 minicomputers that served as the central processors for the DSPR system, the Floating Point Systems Array Processors that performed fast Fourier transforms on data from the alert antennas, and various interface hardware. New hardware installed includes the VAX 4200 minicomputers, CSPI MAP 4000 array processors, and updated interface hardware. All new hardware and associated software were required to interface with the rest of the existing system. The new software was required to replicate all the functions of the existing software.

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The set of documents describes the DSPR system in terms of its current functionality with modernized hardware and software. It will serve as a baseline description from which future specifications for upgrades to hardware and software may be drawn.

1.2 System Overview

The Digital Signal Processing Receiver is a real-time radar data acquisition and analysis system. The function of the NAVSPACECOM Space Surveillance system is to detect, with no prior information, all space objects whose orbits cross the continental United States and to compute their subsequent orbits.

The Space Surveillance system is a multistatic continuous-wave radar system operating as a large radio interferometer, with nine stations located along a great-circle path across the southern United States. The inclination of the great circle is 33.57° with respect to the equator.

The system consists of three transmitters and six receivers. The stations are located as follows:

Transmitters: Jordan Lake Station, Wetumpka, Alabama
Lake Kickapoo Station, Archer City, Texas
Gila River Station, Maricopa, Arizona

Receivers: Tattnall Station, Glennville, Georgia
Hawkinsville Station, Hawkinsville, Georgia (high altitude)
Silver Lake Station, Hollandale, Mississippi
Red River Station, Lewisville, Arkansas
Elephant Butte Station, Truth or Consequences, New Mexico (high altitude)
San Diego Station, Chula Vista, California

Each transmitting station radiates a continuous wave of radio energy that combines with the other transmitting stations' beams to form the Space Surveillance "fence." When an object, such as a satellite, enters the fence, a small fraction of the radio energy is reflected to one or more of the receiver sites. The receiving stations use large multiple-array interferometers to detect the reflected signal and to measure its angle of arrival. The transmitter and receiver arrays are cross-polarized to prevent the transmitted energy from reaching the receivers without having been reflected from a space object. Each receiving station transmits phase and amplitude data, along with frequency identifiers, statistical measures, and time stamps to the Space Surveillance Processing Center via a dedicated telephone line, where local direction angles for each object are computed.

The antenna data available at the receiver stations can be processed to produce three types of data: full-Doppler, half-Doppler, and quarter-Doppler. These three types are also referred to as low-altitude, mid-altitude, and high-altitude, respectively. The output of the full-Doppler data is far more important than either the half- or quarter-Doppler data. For this reason, production of the full-Doppler data by the DSPR system takes priority over half- and quarter-Doppler processing. The purpose, then, of each DSPR is to provide a continuous stream of full-Doppler data to the Space Surveillance Processing Center at Dahlgren, Virginia.

1.3 DSPR System Philosophy

The DSPR system philosophy stems directly from the system purpose. This system is designed to run continuously, with any single component failure resulting in, at most, a very short (less than a

minute) interruption in full-Doppler data processing. For this reason, each DSPR actually consists of two systems that duplicate each other. The primary system normally handles the full-Doppler data from the antennas. The secondary system normally handles the half- and quarter-Doppler data. If the primary system malfunctions and is no longer able to process data, the secondary system detects the failure and declares a "primary system failure." The secondary system then reinitializes itself to become a primary system. This reinitialization process occurs only in the secondary system. If, under normal conditions, the secondary system malfunctions, the primary system detects the failure, but does not attempt to process the half- and quarter-Doppler data. This dual system philosophy is embedded in every aspect of the DSPR system.

1.4 DSPR Subsystems

For the purposes of this document, the DSPR is treated as consisting of the following subsystems. Their functions are briefly described below.

Radio Frequency converts the analog outputs from the antenna arrays to digital form for subsequent processing.

System Monitor and Control initializes all other procedures, controls the system operation, and serves as the interface between the operators and the system.

Utility Bus Control directs and supervises activity on the utility bus and related hardware elements that were designed and developed by NRL.

Target Detection and Selection performs the initial detection of targets that enter the Space Surveillance fence and compiles target lists that are used for target selection. The detection procedure runs in a CSPI MAP 4000 Array Processor; the selection procedure (TRGSEL) runs in the central controller, a DEC VAX 4000 Model 200 (VAX 4200).

Interferometer Data Collection takes the targets selected by the central controller and tunes the digital filters to gather data. Accumulated data is provided to the VAX 4200 for formatting and transmission to the Space Surveillance Processing Center.

Data Processing formats the data collected by the Interferometer Data Collection subsystem for transmission to the Space Surveillance Processing Center.

Data Line Communications is responsible for interfacing the DSPR system to the communications line to the Space Surveillance Processing Center.

Interprocessor Communications provides communications between the central controller of the primary system and that of the secondary system.

Operational Tests (also called OPTESTs) are on-line confidence tests used to exercise one or more components of the DSPR system.

Calibration and Diagnostics allows the operator to check the status of various hardware components of the system. It also generates calibration constants, used to process interferometer data.

The Operational Tests subsystem is not discussed in this document.

2. HARDWARE INTERFACES

The following sections describe the major hardware interfaces both within and among the major subsystems of the DSPR. Figure 1 shows the connectivity between the hardware components.

2.1 Radio Frequency (RF) Subsystem Interfaces

The digital interface to the RF subsystem is the main data bus. The main data bus transports the digital output words from the channel receivers in the RF subsystem for distribution to other subsystems. This parallel bus also passes control and timing signals between the central controller and the timing generator. The data distribution and test card (DD&TC) receives the data and control signals on the bus and distributes the data to the other subsystems.

The 50-pin connectors DATA BUS-0 and DATA BUS-1 on the rear of the channel receivers are the physical interfaces to the main data bus for the primary and secondary systems, respectively. The redundant timing generators interface to the main data bus via connector J1, which is attached by a ribbon cable to the rear of the unit. Precision Connector Designs Connector Part Number (PN) RF25-2852-5 mates with the connectors on the channel receivers and the timing generator. These devices are linked in a daisy-chain to the bus by a 50-pin ribbon cable (Alpha 3580 series), which is bifurcated for connection to the DD&TC. Connectors AJ1 and AJ2 on the DD&TC are 26-pin standard integrated circuit (IC) sockets that mate with T&B/Ansley PN 609-2601M female socket connectors.

The pin assignments (pinouts) on the main data bus are as follows.

Channel Receiver	Timing Generator	DD&TC Connector AJ1	Signal Description
NC *	2,4,6,8	14-17	Ctrl Bits 00-03(Ch Sel)
NC	10	18	Ctrl Bit 04 Mode Control
NC	12	19	1.2-MHz Clock
14	14	20	Ctrl Bit 05 75-kHz Select
NC	18	22	75-kHz S and H Clock
NC,NC	20,22	23,24	Antenna Data Bits 00,01 **
24,26	24,26	25,26	Antenna Data Bits 02,03
odd pins	odd pins	NC	Signal Ground

Channel Receiver	Timing Generator	DD&TC Connector AJ2	Signal Description
28-50 even	28-50 even	14-25	Antenna Data Bits 04-15
odd pins	odd pins	NC	Signal Ground

* NC means not connected.
** These antenna data bits are not active.

The clock signals are necessary for channel identification and recovery. The timing generator derives the 1.2-MHz clock from the 60-MHz signal received from local oscillator #1. The 1.2-MHz clock is a square-wave timing signal used to control the input of data onto the main data bus. The 75-kHz sample-and-hold clock is derived from the 1.2-MHz clock and is used to control the sampling within the analog-to-digital (A/D) converter in the channel receiver. These two clock signals are passed along

with the 14 antenna bits comprising the digitized RF data to the data distribution and test card for distribution to the Interferometer subsystem and the Target Detection and Selection subsystem.

The control signals originate from the central controller and are passed to the DD&TC via the utility bus. The channel select bits identify which antenna channel to use to load data in the test mode. The (test) mode control bit determines the mode by which the timing generator places data on the bus. The "Auto" mode places data from all the channels on the bus in the normal fashion, whereas in the "Load" mode, data from the antenna identified in control bits 0-3 will be placed on all the channels on the bus. The 75-kHz select signal determines which of the 75-kHz clocks from the two systems is to be enabled. This signal is passed to the channel receivers.

2.2 System Monitor and Control Subsystem Interfaces

The primary hardware component in the System Monitor and Control Subsystem is the Digital Equipment Corporation VAX 4000 Model 200 (VAX 4200) minicomputer. The VAX 4200 is the central controller for the DSPR and communicates with external devices via the Qbus. The communications and processing cards that interface the Qbus to external devices have the standard backplane Qbus interface with the VAX 4200. The cards' interfaces with the external devices are described in the following subsections.

2.2.1 Utility Bus Control Subsystem

The DRV1W input/output (I/O) 16-bit parallel interface, in conjunction with a utility bus input/output (UBIO) interface card, provides the interface between the Qbus and the utility bus (UB). The UBIO card is identical to the digital filter input/output (DFIO) card except for the position of jumper J1. The DRV1W[1] has two 37-pin D connectors (J1 and J2) on its front panel. The DRV1W is connected to the UBIO by a 40-conductor ribbon cable. On the DRV1W end is a 3M 37-pin D to ribbon connector PN 3485-2400, and on the UBIO end (J1 and J2) are female Bergcon-type connectors. Because the utility bus cards were originally designed to interface with a Unibus DR11-K, the UBIO is required to generate control signals for the DRV1W and the utility bus cards. The UBIO is connected to the utility bus by two 40-conductor ribbon cables (J3 and J4) with female Bergcon connectors on the UBIO end and a low-profile, 40-contact DIP plug such as T&B/Ansley PN 609-M407H, which plugs into connector areas BG1 and BG31 on the data distribution and test card. The pin assignments for J1-J3 and J2-J4 of the UBIO are given in Tables 1 and 2. The high byte of the 16-bit data word is defined as the UB card address. The low byte contains the data pertaining to the addressed device.

[1] *DRV11-WA General Purpose DMA Interface*, DEC User's Guide EK-DRVWA-UG-002, 1986.

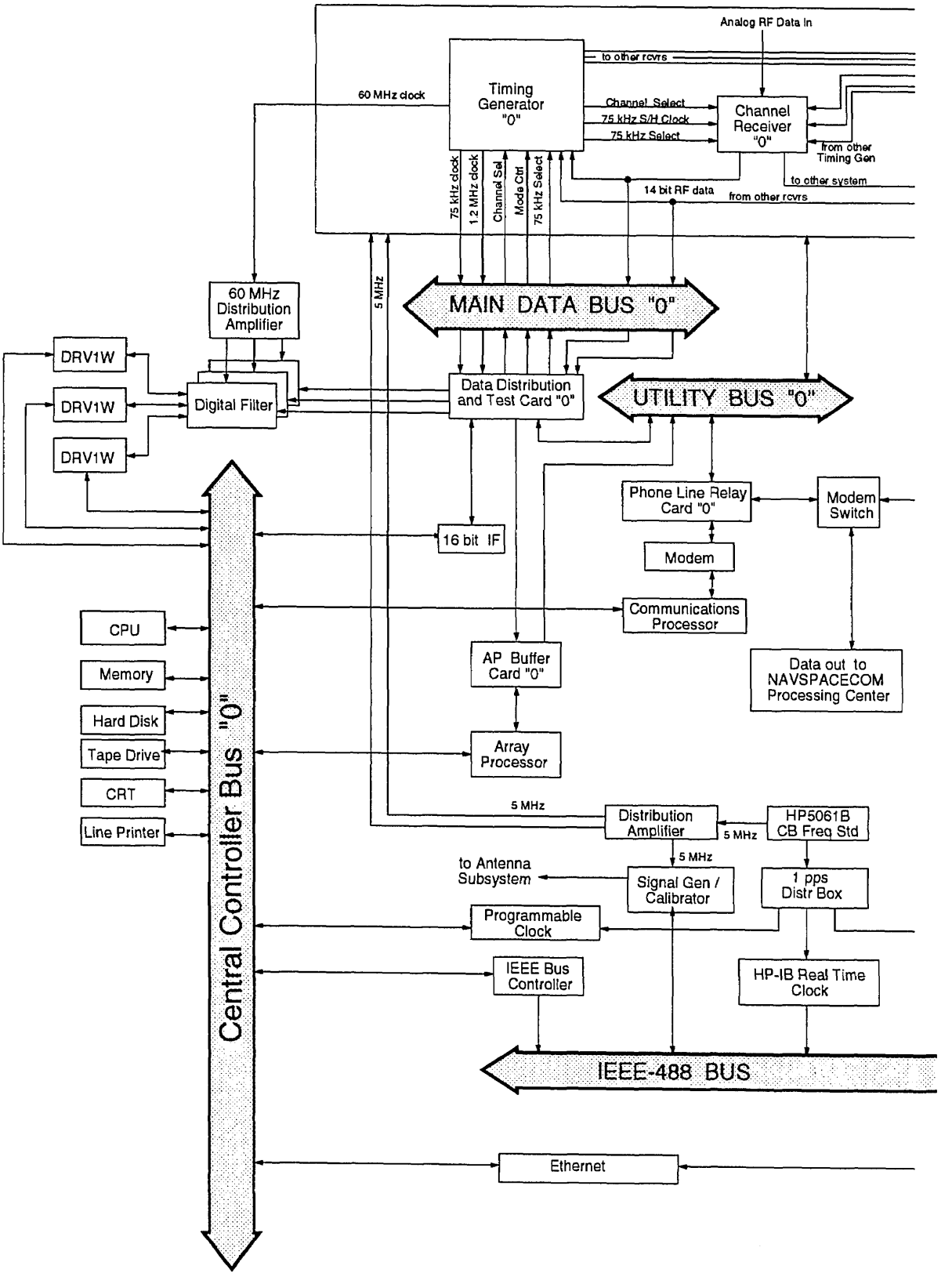


Fig. 1—DSPR components diagram

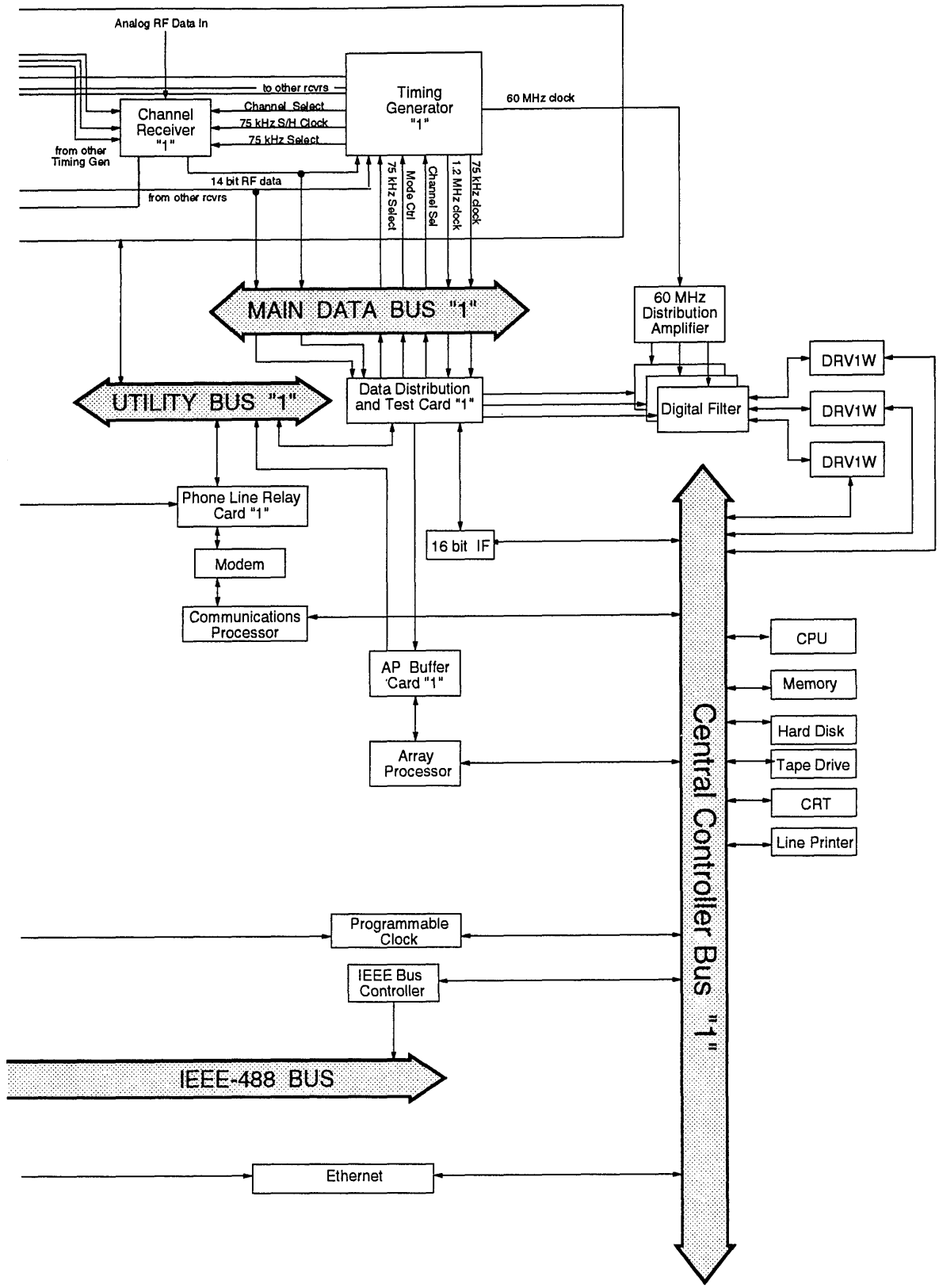


Fig. 1—DSPR components diagram

Table 1 — Utility Bus I/O Card Connections for J1 and J3

Conn J1		Conn J3
Pin	**Signal Description**	**Pin**
1	Ground	
3	Cycle Req H	U3-5
5	Ground	
7	Init V2 H	Open
9	Ground	
11	Ready H	U1-5
13	Ground	
15	WC Inc Enb H	Open
17	Single Cycle	Open
19	Status A H	U1-8
21	Ground	
23	Init H	Ground
25	Ground	
27	Status B H	Open
29	Ground	
31	Status C H	Open
33	Ground	
35	Ground	
37	Ground	
2	Ground	

Conn J1		Conn J3
Pin	**Signal Description**	**Pin**
4	Ground	
6	OUT 07	23
8	OUT 08	25
10	OUT 06	21
12	OUT 09	27
14	OUT 05	19
16	OUT 10	29
18	OUT 04	17
20	OUT 11	31
22	OUT 03	15
24	OUT 12	33
26	OUT 02	13
28	OUT 13	35
30	OUT 01	11
32	OUT 14	37
34	OUT 00	9
36	OUT 15	39
38	Open	
39	Open	
40	Open	

Table 2 — Utility Bus I/O Card Connections for J2 and J4

Conn J2		Conn J4
Pin	**Signal Description**	**Pin**
1	Ground	
3	Busy H	U1-3
5	Ground	
7	Attention H	Ground
9	Ground	
11	A 00 H	Ground
13	Ground	
15	BA Inc Enb H	Open
17	Ground	
19	Funct 3 H	U4-2
21	Ground	
23	C0 H	Ground
25	Ground	
27	Funct 2 H	U1-11
29	Ground	
31	C1 H	U1-2
33	Ground	
35	Funct 1 H	U1-1
37	Ground	
2	Ground	

Conn J2		Conn J4
Pin	**Signal Description**	**Pin**
4	Ground	
6	IN 07	18
8	IN 08	16
10	IN 06	20
12	IN 09	14
14	IN 05	22
16	IN 10	12
18	IN 04	24
20	IN 11	10
22	IN 03	26
24	IN 12	8
26	IN 02	28
28	IN 13	6
30	IN 01	30
32	IN 14	4
34	IN 00	32
36	IN 15	2
38	Open	
39	Open	
40	Open	

The following paragraphs describe the operation of utility bus and DRV1W control signals.

Utility Bus Control Signals: The input control bit "Internal Data Accept" indicates that the central controller has accepted the data on the utility bus. The output bit "External Data Ready" indicates that the utility bus has data available for the central controller. The command data are directed to the utility bus device addressed in the command address bits. The two output control bits, "Internal High Data Ready" and "Internal Low Data Ready," indicate that the DRV1W has data available for the utility bus. "Internal High Data Ready" indicates that the eight most significant bits (high byte) of DRV1W data are on the utility bus. "Internal Low Data Ready" indicates that the eight least significant bits (low byte) of DRV1W data are on the utility bus. The input bit "External Data Accept" indicates that the addressed device has accepted the data on the utility bus.

DRV1W Control Signals: The DRV1W control signals are "Ready," "Busy," "C0 and C1," and "Cycle Request." Transfers are controlled by the user device. There are three function bits which can be set by the DRV1W and three status bits which can be set by the user and read by the DRV1W. The direction of the transfer is determined by C1 with C0 held high. C1 is set high for a transfer into the DRV1W from the UB; it is set low for a write to the UB. Function bit F1 is used to control the value of C1.

Theory of Operation: For a transfer to the UB, function bits 1, 2, and 3 are set. Function bit 1 is returned through an inverter as "C0" and also enables "Load High Data." Function bit 2 enables the "Ready" signal as the input to an SN74123 dual monostable multivibrator, or single shot. Function bit 3 enables "Load Low Data." After the function bits are set, the DRV1W sets "Ready" low to indicate it is ready for a transfer. Ready is passed to an SN74123 dual single shot. The output is sent to the DRV1W as "Cycle Request." The DRV1W sends "Busy," which is passed to the UB as "Load Low Data" and "Load High Data." Each card on the UB compares the address byte to its own address, which is set by switches. If they match, the card loads the data byte into its data register. It also passes the load signal back on the bus as "External Data Accepted." The "Busy" signal also enables the other single shot, whose output is passed to the UB as "Internal Data Accepted" and to the A input of the first single shot to start another "Cycle Request" pulse. When the transfer is complete, "Ready" is asserted high.

For a transfer from a card on the UB, first a write cycle is performed with only function bits F1 and F2 set. The "Load High Data" signal generated from F1 and the output of the second single shot forces the addressed card to place its data and address on the bus. Then a read is performed with all function bits clear. The DRV1W stores the data on the bus in the VAX 4200 memory.

2.2.2 Target Detection and Selection Subsystem

The CSPI MAP 4000 array processor consists of four boards: a host interface (HINT) board, a CPU board, a main memory board, and a direct input/output (DIO) interface board. The DIO is modeled on the DEC DRV1W 16-bit parallel interface card. The MAP 4000 plugs into the VAX 4200 chassis. The Qbus HINT board provides the translation and handshaking signals needed between the VAX 4200 and the host interface in the array processor. The MAP 4000 is totally software controlled by the central controller via the host interface. A custom array processor input/output (APIO) card is used to select alert antenna data from the main data bus and pass it to the DIO for entry into the MAP 4000.

2.2.3 Interferometer Subsystem

The Interferometer subsystem consists of three digital filters (DFs). A DRV1W/DFIO combination is responsible for data transfer and control between each DF and the central controller. The following paragraphs describe the operation of digital filter and DRV1W control signals.

Digital Filter Control Signals: The input control bit "Internal Data Accept" indicates that the central controller has accepted data from the DF. The output bit "External Data Ready" indicates that the DF has data available for the central controller. The command data are directed to the DF register addressed in the command address bits. The output control bit "Internal High Data Ready" indicates that the DRV1W has data available for the DF. This bit is returned by the DF as input bit "External Data Accept" to indicate that the DF has accepted the data.

DRV1W Control Signals: The DRV1W control signals are "Ready," "Busy," "C0 and C1," and "Cycle Request." Transfers are controlled by the user device. There are three function bits which can be set by the DRV1W and three status bits which can be set by the user and read by the DRV1W. The direction of the transfer is determined by C1 with C0 held high. C1 is set high for a transfer into the DRV1W from the DF and low for a write to the DF. Function bit F1 is used to control the value of C1.

Theory of Operation: For a transfer to the DF, function bits 1 and 2 are set. Function bit 1 is returned through an inverter as "C0" and also enables "Load High Data." Function bit 2 enables the "Ready" signal as the input to a single shot. After the function bits are set, the DRV1W sets "Ready" low to indicate it is ready for a transfer. "Ready" is passed to an SN74123 dual single shot. The output is sent to the DRV1W as "Cycle Request." The DRV1W sends "Busy," which is passed to the DF as "Load High Data." The DF loads the data into the register indicated by the address bits of the input word and returns "High Data Ready" as "External Data Accepted." The "Busy" signal also enables the other single shot, whose output is passed to the DF as "Internal Data Accepted." "External Data Accepted" is passed to the A input of the first single shot to start another "Cycle Request" pulse. When the transfer is complete, "Ready" is asserted high, which inhibits "Cycle Request."

For a transfer from the DF, a read is queued with the function bits cleared. Function bit 1 is inverted and is returned as "C0" to indicate a read. Function bit 2 being clear enables "External Data Ready" as the trigger for the first single shot. After the DF has completed a discrete Fourier transform (DFT), it places its first data word on the DRV1W input lines and sets "External Data Ready," which initiates a "Cycle Request." "Busy" is set by the DRV1W and passed to the DF as "Internal Data Accepted." The DF places the next data word on the input bus on the trailing edge of "Busy" and initiates an "External Data Accepted" pulse. This signal enables the first single shot, and another "Cycle Request" is generated. After all the data from the DFT has been transmitted (56 16-bit words), "Data Ready" is cleared and the system waits for another DFT to be completed.

2.2.4 Data Line Communications Subsystem

The Codex V.3225 modem interfaces to the central controller via the DSV11 synchronous interface using a standard RS-232C interface. The DSV11 has two independent channels, of which the DSPR system uses channel 0. Connector J0 on the DSV11 is a 50-pin male D connector. An 8-foot 50-pin to 25-pin cable adapts the output to an RS-232C 25-pin male connection which runs to J4 of the junction panel. A 15-foot 25-pin male-to-female cable connects the junction panel J4 to the modem.

The following signals are active:

Transmit Data (TD)	Receive Data (RD)
Transmit Clock (TC)	
Receive Clock (RC)	
Data Terminal Ready (DTR)	DCE Receiver Ready (DSR)
Request to Send (RTS)	Clear to Send (CTS)
Carrier Detect (RLSD)	
Ring Indicator (RI)	
External Transmit Clock (ETC)	

2.2.5 Interprocessor Communications Subsystem

The Interprocessor Communications subsystem (ICC) uses the Ethernet controller imbedded on the CPU card of the VAX 4200. The VAX 4200 has both a thickwire and thinwire connection. The DSPR system uses only the thinwire connection. A coaxial cable with male BNC connectors runs from the thinwire connection on the CPU front panel to J7 of the junction panel, which has a BNC feed-through connector. A 30-foot BNC male-to-male cable connects J7 of the two junction panels.

2.2.6 Calibration and Diagnostics Subsystem

The Qbus interface to the IEEE-488 bus is the IEQ11 bus controller. The controller has two independent channels, of which only channel 1 is used by the DSPR system. Connector J1 on the IEQ11 is a standard IEEE 24-pin connector.

2.2.7 Operator's Console

The operator's console consists of a VT240 video terminal and a LA120 line printer for each system. The LA120 is used as the VAX 4200 console and is connected to the console jack on the VAX 4200 CPU front panel, which is a DEC-423 modular jack. An 8-foot cable with a DEC-423 MMJ connector on one end and a 9-pin D connector on the other connects the console to the junction panel. The VT420 is connected to line 0 of a DZQ11 four-line RS-232C communications card. The DZQ11 has four 9-pin D connectors (one for each line) on its front panel. An 8-foot cable with 9-pin male and female connectors runs from the DZQ11 to the junction panel. Both the LA120 and VT240 run at 9600 baud.

2.2.8 System Timing

The 1-pulse-per-second (pps) distribution box interfaces to the central controller via the KWV11 programmable real-time clock. The KWV11 clock is used to obtain precise time for time stamping the observed data. The 1-pps signal is used to reset the counter in the clock. A coaxial cable with BNC connectors runs from the distribution box to the Schmitt trigger 2 input of a UDIP-KW front panel, which is located in the rear of the VAX 4200 rack. A cable with 25-pin D connectors runs from the UDIP-KW to the KWV11 front panel.

The KWV11 interrupts the central controller to update the system clock based on the 1-pps from the cesium time standard. Upon receiving the interrupt, the connect-to-interrupt code updates the system time.

2.3 Utility Bus Control Subsystem Interfaces

The utility bus is used to initialize the custom hardware in the DSPR system and to detect changes in the hardware during system operation. As shown in Fig. 2, the hardware devices on the bus are linked in a daisy-chain, and each has a specific address. The bus is 20 bits wide in each direction, consisting of eight bits of data, eight bits of addressing, and control signals.

The utility bus word is 16 bits long. The eight most significant bits (high byte) contain the address of the device (card). The eight least significant bits (low byte) contain the command or status data relating to the device. Data from the central controller to the utility bus consists of commands to enable/disable or change hardware features of the addressed device. Data to the central controller from the utility bus describe changes in hardware settings of the device associated with the address.

The utility cards connect to the VAX 4200 through the fourth DRV1W on the Qbus and its associated UBIO card. The connectors on the UBIO are associated in pairs. J1 and J3 contain the output lines that handle commands to the UB cards, and J2 and J4 contain the input lines to the DRV1W. Control signals for the DRV1W and the UB are also on these connectors. Table 1 shows the UBIO connections for J1 and J3. Table 2 shows the connections for J2 and J4. J3 on the UBIO is connected by a 40-conductor ribbon cable to Bergcon connector J6 on the APIO card. The signal is passed through to the 40-pin Bergcon connector J3. A 40-pin ribbon cable connects J3 on the APIO card to area BG31 on the DD&TC. A low-profile, 40-contact DIP plug T&B/Ansley PN 609-M407H is used to plug into connector area BG31 on the DD&TC. Table 3 gives the pinouts of this cable. The cards are daisy-chained on the utility bus and the bus is looped back to the input to the DRV1W. The APIO is not on the input chain because it cannot return data to the VAX 4200. Table 4 gives the pinouts for the cable from area BG1 on the DD&TC to connector J4 on the UBIO card.

The signal descriptions for the command status module (CSM) connections are given in Section 2.2.1.

2.3.1 System Monitor and Control Subsystem

The DRV1W is connected to the utility bus via the data distribution and test card. This connection is shown in Fig. 2 and described in Section 2.2.1.

2.3.2 Data Distribution and Test Card

The DD&TC is the interface between the RF subsystem, the Target Detection and Selection subsystem, and the Interferometer subsystem. The DD&TC distributes data under control of the central controller. Figure 3 shows the connector interfaces to the various subsystems.

Incorporated into this card are the CSM functions and connections to the bus with pin assignments as detailed in the previous section.

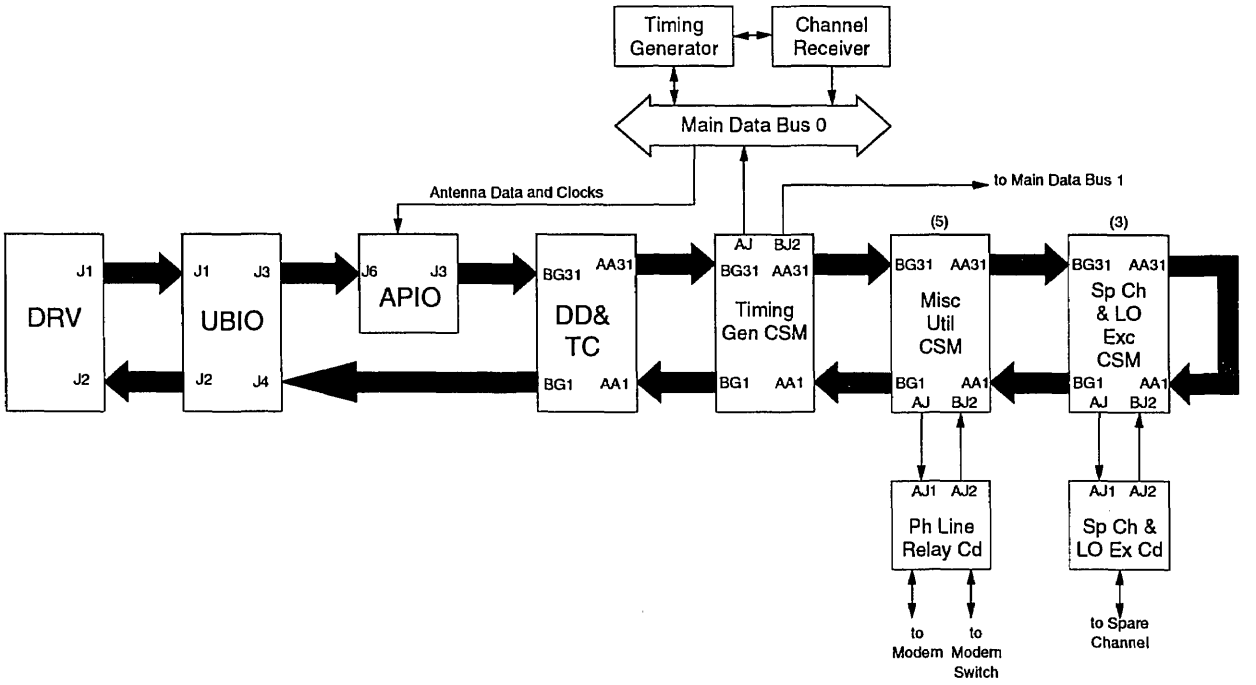


Fig. 2 — Utility bus block diagram

Table 3 — Array Processor I/O Card Connections for J3 and BG31

Conn J3		BG31
Pin	**Signal Descr.**	**Pin**
1		40
2	Ground	1
3	Ext Data Accept	39
4	Ground	2
5	Load High Data	38
6	Ground	3
7	Load Low Data	37
8	Ground	4
9	OUT 00	36
10	Ground	5
11	OUT 01	35
12	Ground	6
13	OUT 02	34
14	Ground	7
15	OUT 03	33
16	Ground	8
17	OUT 04	32
18	Ground	9
19	OUT 05	31
20	Ground	10

Conn J3		BG31
Pin	**Signal Descr.**	**Pin**
21	OUT 06	30
22	Ground	11
23	OUT 07	29
24	Ground	12
25	OUT 08	28
26	Ground	13
27	OUT 09	27
28	Ground	14
29	OUT 10	26
30	Ground	15
31	OUT 11	25
32	Ground	16
33	OUT 12	24
34	Ground	17
35	OUT 13	23
36	Ground	18
37	OUT 14	22
38	Ground	19
39	OUT 15	21
40	Ground	20

Table 4 — Utility Bus I/O Card Connections for BG1 and J4

BG1		J4
Pin	**Signal Descr.**	**Pin**
1	IN 15	2
2	IN 14	4
3	IN 13	6
4	IN 12	8
5	IN 11	10
6	IN 10	12
7	IN 09	14
8	IN 08	16
9	IN 07	18
10	IN 06	20
11	IN 05	22
12	IN 04	24
13	IN 03	26
14	IN 02	28
15	IN 01	30
16	IN 00	32
17	Int Data Ready	34
18	Int Data Ready	36
19	Int Data Accept	38
20	Initiate	40

BG1		J4
Pin	**Signal Descr.**	**Pin**
21	Ground	40
22	Ground	38
23	Ground	36
24	Ground	34
25	Ground	32
26	Ground	30
27	Ground	28
28	Ground	26
29	Ground	24
30	Ground	22
31	Ground	20
32	Ground	18
33	Ground	16
34	Ground	14
35	Ground	12
36	Ground	10
37	Ground	8
38	Ground	6
39	Ground	4
40	Ground	2

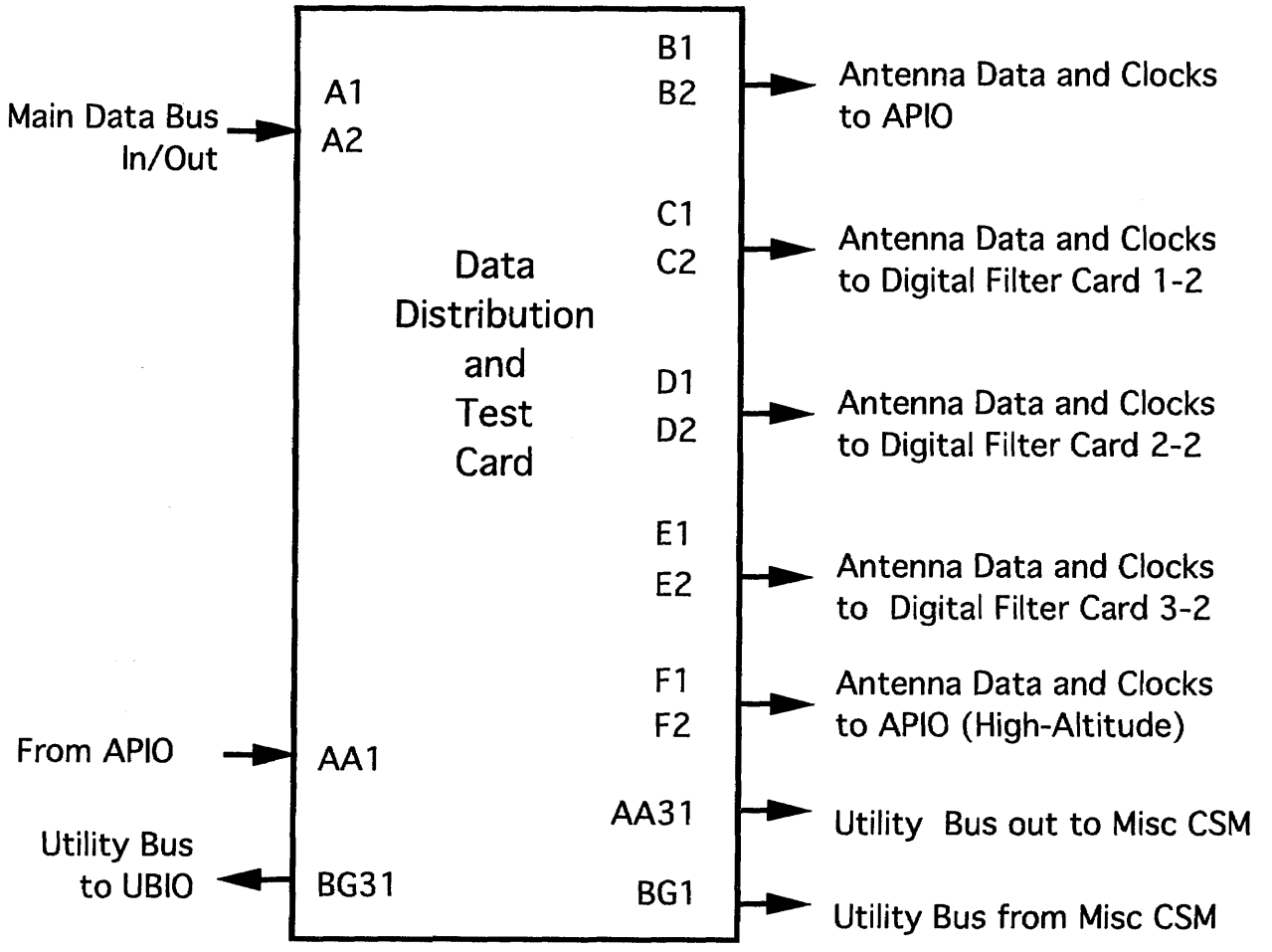


Fig. 3 — Data Distribution and Test Card connections

The command data bits to the DD&TC on connector area BG31 are as follows.

Command Data Bit 0-3	Channel Select
Command Data Bit 4	Mode Control
Command Data Bit 5	75-kHz Select
Command Data Bit 6	Interrupt Control
Command Data Bit 7	Test Mode

The command data passed to the DD&TC consist of initializing data for the timing generator and test mode commands for both the timing generator and the DD&TC. Section 2.1 discusses the channel select, mode control, and 75-kHz select commands. The Interrupt Control bit determines whether the DD&TC will generate interrupts to the central controller at a rate of 75 kHz. To prevent overloading the central controller, this bit is normally disabled.

The test mode bit controls whether the DD&TC is in test mode. The test mode is used for off-line diagnostics. When this bit is 1 (test mode), the DD&TC generates and sends test data to the other subsystems in place of the antenna data. Test data can take the form of a sine wave at a variable frequency, a ramp, or a constant (DC) level. The sine wave and the ramp may each be applied to one channel, all channels, or none. The DC level may be applied to one channel, all channels except one, all channels, or none. The data bits determine which channels receive the test data.

While the DD&TC is in test mode, it does not use address 011. Instead, the address given identifies the type of test data to generate. Logically, the test card functions are separated from the DD&TC and each other and appear as separate cards. Physically, the system is disconnected from the data distribution function of the DD&TC and is latched into the function generator.

The addresses for the test patterns are as follows.

Card Number (octal)	Function
012	Least significant byte for the sine wave frequency
013	Most significant byte for the sine wave frequency
014	Least significant byte for the constant (DC) level
015	Most significant byte for the constant (DC) level
016	Least significant byte for the control signal (ramp)
017	Most significant byte for the control signal (ramp)

There are no outputs from the DD&TC to the central controller.

2.3.3 Target Detection and Selection Subsystem

The APIO card has an input utility bus interface with the data distribution and test card and an output bus interface with the miscellaneous utility CSM card. Low profile, 40-contact DIP T&B/Ansley PN 609-M407H connectors plug into connector areas AA31 and AD31 to provide the pin assignments as follows.

Pin #	APIO In/Out AA31	AD31	Signal Description
21-28	in	out	Command Address Bits 07-00
29-32	in	out	Command Data Bits 7-4 (Bfr Size)
33-36	in	out	Command Data Bits 3-0 (Chan Sel)
37	in	out	Internal Low Data Ready
38	in	out	Internal High Data Ready
39	out	in	External Data Accepted

The command data forwarded to the APIO from the central controller consist of channel select bits. The channel select bits are the alert channel identification that selects which receiver channel outputs are to be analyzed by the array processor.

2.3.4 Phone Line Relay Card

The phone line relay card is the interface for the alarms, transmit and receive lines, and power supply monitor lines. It sends alarms and status reports to the central controller via the utility bus. It connects to the utility bus via its CSM, the miscellaneous utility CSM card. The connectors AJ1, AJ2, BJ1, and BJ2 for both cards are 26-pin standard IC sockets that mate with T&B/Ansley PN 609-2601M female socket connectors. The pin assignments for the connectors on the phone line relay card are shown below.

Connector AJ1: This connector interfaces with connector AJ1 (System 0) or AJ2 (System 1) on the CSM card. The pin assignments are the same for all connectors and are as follows.

Pin #	Phone Relay Card Input/Output	Signal Description
1	in	Data Bit 0 (Cal Relay Control)
2	in	Data Bit 1 (Phone Relay)
3	in	Data Bit 2 (Alarm 1)
4	in	Data Bit 3 (Alarm 2)
5	in	Data Bit 4 (Cal Type)
6-8	in	Data Bits 5-7 (not used)
9	in	Strobe
10	in	FF
11	out	FF
14-26		Signal Ground

The phone relay signal controls the switching to connect the modem to the phone line. The modem of the primary system (identified in bit 2) is connected to the phone line, and the modem of the secondary system is placed in a loop-back mode. If the phone line relay card for both systems is set in standby, both the modems and the phone line will be placed in a loop-back mode. The "Alarm 1" signal to the phone line relay card is sent to the alarm box to energize the lamp. The "Alarm 2" signal

energizes the buzzer that is connected to the alarm box. "Cal Relay Control" and "Cal Type" were two signals associated with the calibrator in the production (old) receiver system. "Cal Relay" controlled the switching between the production calibrator and the modernization (current) calibrator. "Cal Type" indicated whether the calibration signal was at the designated reference threshold. These two signals are obsolete since the production calibrator is no longer in use and the current calibrator is controlled by the IEEE-488 bus. This signal information is given here for clarification.

Connector AJ2: This connector interfaces with connector BJ2 on the CSM card. The pin assignments are the same for both connectors and are as follows.

Pin #	Phone Relay Card Input/Output	Signal Description
1	out	Data Bit 0 (Prod Cal)
2	out	Data Bit 1 (Screen Room Door Open Alarm)
3	out	Data Bit 2 (Fire Detection Alarm)
4	out	Data Bit 3 (Screen Room High Temp Alarm)
5	out	Data Bit 4 (Pwr Supply Degradation Alarm)
6	out	Data Bit 5 (not used)
7	out	Data Bit 6 (Communications Switch)
8	out	Data Bit 7 (CPU Number)

The door, fire, and temperature alarms are data bits initiated by the alarm sensors and forwarded to the central controller. Power supply degradation is based on sampling the +12, +24, +28, and -24 volt power supply voltages from both systems. An alarm is forwarded if any one of the eight voltages falls below its minimum allowable value. Originally, the "Prod Cal" signal indicated whether the production calibrator was on or off. Presently, this signal is used as a dehydrator (humidity) alarm. The Communications Switch signal identifies which modem is connected to the phone line, and the CPU number signal indicates the CPU to which the phone line relay card is connected.

2.3.5 Spare Channel and Local Oscillator (LO) Exchange Card

The Spare Channel and LO Exchange Card connects to the utility bus via its CSM, the Spare Channel and LO Exchange CSM Card. The connectors AJ1, AJ2, BJ1, and BJ2 for both cards are 26-pin standard IC sockets that mate with T&B/Ansley PN 609-2601M female socket connectors with connections as shown below.

Connector AJ1: This connector interfaces with connector AJ1 (System 0) or AJ2 (System 1) on the CSM card. The pin assignments are the same for all connectors and are as follows.

Pin #	Spare Ch & LO Ex Input/Output	Signal Description
1-4	in	Data Bits 0-3 (Chan Sel)
5	in	Data Bit 4 (LO 1 Sel)
6	in	Data Bit 5 (LO 2 Sel)

Connector AJ2: This connector interfaces with connector BJ2 on the CSM card. The pin assignments are the same for both cards and are as follows.

Pin #	Spare Ch & LO Ex Input/Output	Signal Description
1	out	Data Bit 0 (LO 1 "0" Status)
2	out	Data Bit 1 (LO 1 "1" Status)
3	out	Data Bit 2 (LO 1 Sel)
4	out	Data Bit 3 (LO 2 "0" Status)
5	out	Data Bit 4 (LO 2 "1" Status)
6	out	Data Bit 5 (LO 2 Sel)

The channel select bits form a four-bit data word that indicates which antenna channel the spare channel switch shall select for the spare channel receiver. The input "LO Select" bits control whether the "0" or "1" oscillator circuit will be used for each local oscillator. The output "LO Status" bits provide the status of the local oscillator circuits. The output "LO Select" indicates the decision made by the spare channel and LO exchange card based on the "LO Select" command from the central controller and the status of the circuit.

2.4 Target Detection and Selection Subsystem Interfaces

The primary hardware components of the Target Detection and Selection subsystem are the CSPI MAP 4000 array processor and the APIO interface card. The System Monitor and Control interface is described in Section 2.2.2 and the Utility Bus Control interface is described in Section 2.3.3.

2.4.1 Data Distribution and Test Card

The APIO card provides two interfaces between the subsystem and the DD&TC. The utility bus interface is described in Section 2.3.3. The data interface to the APIO consists of alert channel data from the continuous stream of antenna data passing through the DD&TC. The APIO extracts this data and transfers it to the MAP 4000 in 16-bit words. The connectors on the DD&TC are 26-pin standard IC sockets which mate with T&B/Ansley PN 609-2601M female socket connectors. The connectors on the APIO card are 26-pin Bergcon-type connectors. The APIO card is connected to the MAP DIO board through two 40-pin ribbon connectors with Bergcon-type connectors. By using the 75-kHz and 1.2-MHz clocks, the APIO determines when the data from the particular RF channel, input through the utility bus, is on the main data bus. It latches the data and passes it to the DIO for input into memory in the MAP 4000.

The pin assignments are the same for both cards.

Connector BJ1 on DD&TC to J1 on AP Card

Pin #	Signal Description
19	1.2-MHz Clock
22	75-kHz Clock
* 23-26	Antenna Data Bits 0-3

*The two least significant bits contain no RF data and are always 1.

Connector BJ2 on DD&TC to J2 on APIO Card

Pin #	Signal Description
14-25	Antenna Data Bits 4-15

2.4.2 APIO to DIO

The APIO is connected to the MAP through a CSPI DIO 16-bit parallel interface card. The DIO emulates the DEC DRV11 and performs similarly. J4 and J5 on the APIO card are connected to J4 and J5, respectively, on the DIO board by a 40-conductor ribbon cable with 40-pin Bergcon-type female connectors on each end.

2.5 Interferometer Subsystem Interfaces

The primary hardware components of this subsystem are the digital filters. The digital filters are two-card units. Digital filter card 1 is the control card and interfaces with the VAX 4200 through a DRV1W 16-bit parallel interface. Digital filter card 2 performs the DFTs on the antenna signals and interfaces with the DRV1W and the DD&TC.

2.5.1 Data Distribution and Test Card / Digital Filter Interface

Digital filter card 2 receives the antenna data and timing signals from the DD&TC. The connectors on both cards are 26-pin standard IC sockets that mate with T&B/Ansley PN 609-2601M female socket connectors. Connectors CJ1, DJ1, and EJ1 interface with connector DJ1 on digital filter card 1-2, 2-2, and 3-2, respectively. Connectors CJ2, DJ2, and EJ2 interface with connector DJ2 on digital filter card 1-2, 2-2, and 3-2, respectively. The pin assignments are the same for both the DD&TC connectors and their respective digital filter card connectors.

Connectors CJ1, DJ1, and EJ1 on DD&TC to DJ1 on digital filter card 2

Pin #	Signal Description
19	1.2-MHz Clock
22	75-kHz Clock
* 23-26	Antenna Data Bits 0-3

*The two least significant bits contain no RF data and are always 1.

Connectors CJ2, DJ2, and EJ2 on DD&TC to DJ2 on digital filter card 2

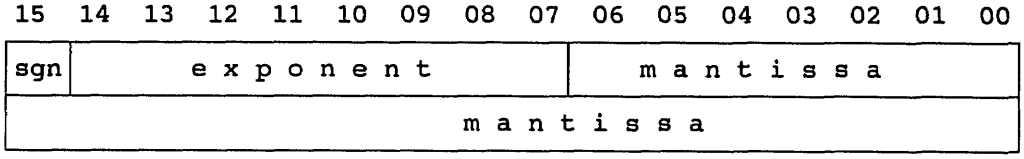
Pin #	Signal Description
14-25	Antenna Data Bits 4-15

2.5.2 Digital Filter / VAX 4200 Interface

The DRV1W is responsible for transferring data between the VAX 4200 and the digital filters. Each DF is connected to its DFIO/DRV1W pair. The DFIOs are identical to the UBIO, and the connections are given in Tables 1 and 2.

DRV1W Output Commands to the DF: Connector J3 on the DFIO is a 40-pin male DuPont Bergcon PN 1209941-02. A mating female Bergcon connector is attached to a 40-conductor ribbon cable, which is bifurcated at the other end and terminated into two 26-pin T&B/Ansley PN 609-2601M female socket connectors. The 26-pin connectors mate with the standard IC sockets on the digital filter cards at locations DJ1 and DJ2. The pin assignments are given in Table 5.

DF Input Data to the DRV1W: The data transferred from digital filter card 2 are the outputs of the DFTs performed at the Doppler frequency of the selected target. For each target, a DFT is performed on each antenna channel at up to 55 time frames. The real and imaginary components of the DFT output both have a range less than $|1.0|$ and consist of two 16-bit words. Prior to transmission to the DRV1W, the card converts the DFT outputs from a two's complement integer format to the standard single precision floating point format of VAX 4200 Fortran. This conversion is done for each component by adding a bias of three, which results in a number with a fixed sign and exponent. The sign and exponent are hardwired in the card to create a normalized floating point word in the F-floating format of VAX 4200 Fortran, which is:



The results are sent to the DRV1W for channels 0-13 in this eight-byte order:

Word 1:	8 bits exponent real (IN00-07)
	1 bit sign, 7 bits mantissa real (IN08-15)
Word 2:	16 bits mantissa real (IN00-15)
Word 3:	8 bits exponent imaginary (IN00-07)
	1 bit sign, 7 bits mantissa imaginary (IN08-15)
Word 4:	16 bits mantissa imaginary (IN00-15)

A 40-conductor ribbon cable runs between areas DJ1 and DJ2 on DF card 1 to connector J4 on the DFIO card. At the DF end the 40-conductor ribbon cable is bifurcated and terminated into two 26-pin T&B/Ansley PN 609-2601M female socket connectors. The 26-pin connectors mate with the standard IC sockets on the digital filter cards at locations DJ1 and DJ2. On the DFIO end is a 40-pin female Bergcon connector, which plugs into J4, a 40-pin male DuPont Bergcon PN 1209941-02. Table 6 gives the pin assignments.

This interface carries the commands required to control the digital filters. The high byte of the 16-bit word is used to select the function. The low byte contains the setup data for the function.

The filter command functions are as follows.

Function	OUT12-OUT08 Bit Sequence	OUT00-OUT07 Function Setup Data
Load low byte freq	00000	target freq (low byte)
Load high byte freq	00001	target freq (high byte)
Load low byte bndwth	00010	# samples (low byte)
Load high byte bndwth	00011	# samples (high byte)
Reset this filter and next filter	00100	not used
Reset this filter and previous filter	00101	not used
Reset this filter only	00110	not used
Reset all 3 filters	00111	not used
Unused	01000-11110	
No-op	11111	not used

The command flow to the filter begins with setting the bandwidth. This corresponds to the number of antenna data samples to be used in the DFT. Next the frequency is set; this corresponds to the Doppler bin number of the target. The high bits are loaded first so that the frequency can be easily retuned to track the Doppler rate by readjusting the low bits. Setting the bandwidth and frequency functions both require two 16-bit transfers for each 16 bits of data. The reset functions command the filter to clear all accumulated data and to begin a new integration cycle. The no-op words are ignored by the digital filter and are used as filler words to increase the output buffer length of the DRV1W.

The control signals are described in Section 2.2.1.

Table 5 — Digital Filter I/O Card Connector J3

Conn J3

Pin	Signal Descr.	Pin
1	Initiate	DJ1-1
2	Ground	DJ1-26
3	Ext Data Accept	DJ1-2
4	Ground	DJ1-25
5	Load High Data	DJ1-3
6	Ground	DJ1-24
7	Load Low Data	DJ1-4
8	Ground	DJ1-23
9	OUT 00	DJ1-5
10	Ground	DJ1-22
11	OUT 01	DJ1-6
12	Ground	DJ1-21
13	OUT 02	DJ1-7
14	Ground	DJ1-20
15	OUT 03	DJ1-8
16	Ground	DJ1-19
17	OUT 04	DJ1-9
18	Ground	DJ1-18
19	OUT 05	DJ1-10
20	Ground	DJ1-17

Conn J3

Pin	Signal Descr.	Pin
21	OUT 06	DJ1-11
22	Ground	DJ1-16
23	OUT 07	DJ1-12
24	Ground	DJ1-15
25	OUT 08	DJ1-13
26	Ground	DJ1-14
27	OUT 09	DJ2-1
28	Ground	DJ2-26
29	OUT 10	DJ2-2
30	Ground	DJ2-25
31	OUT 11	DJ2-3
32	Ground	DJ2-24
33	OUT 12	DJ2-4
34	Ground	DJ2-23
35	OUT 13	DJ2-5
36	Ground	DJ2-22
37	OUT 14	DJ2-6
38	Ground	DJ2-21
39	OUT 15	DJ2-7
40		DJ2-20

Table 6 — Digital Filter I/O Card Connector J4

Conn J4

Pin	Signal Descr.	Pin
1	Ground	CJ1-13
2	IN 15	CJ1-14
3	Ground	CJ1-12
4	IN 14	CJ1-15
5	Ground	CJ1-11
6	IN 13	CJ1-16
7	Ground	CJ1-10
8	IN 12	CJ1-17
9	Ground	CH1-9
10	IN 11	CJ1-18
11	Ground	CJ1-8
12	IN 10	CJ1-19
13	Ground	CJ1-7
14	IN 09	CJ1-20
15	Ground	CJ1-6
16	IN 08	CJ1-21
17	Ground	CJ1-5
18	IN 07	CJ1-22
19	Ground	CJ1-4
20	IN 06	CJ1-23

Conn J4

Pin	Signal Descr.	Pin
21	Ground	CJ1-3
22	IN 05	CJ1-24
23	Ground	CJ1-2
24	IN 04	CJ1-25
25	Ground	CJ1-1
26	IN 03	CJ1-26
27	Ground	CJ2-13
28	IN 02	CJ2-14
29	Ground	CJ2-12
30	IN 01	CJ2-15
31	Ground	CJ2-11
32	IN 00	CJ2-16
33	Ground	CJ2-10
34	Dev Data Ready	CJ2-17
35	Ground	CJ2-9
36	Dev Data Ready	CJ2-18
37	Ground	CJ2-8
38	Dev Data Accepted	CJ2-19
39	Ground	CJ2-7
40	Initiate	CJ2-20

2.6 Data Line Communications Subsystem Interfaces

The single hardware interface for this subsystem is described in Section 2.2.4.

2.7 Interprocessor Communications Subsystem Interfaces

The single hardware interface for this subsystem is described in Section 2.2.5.

2.8 Calibration and Diagnostics Subsystem Interfaces

The primary hardware component of this subsystem is the Hewlett-Packard (HP) 8565A Signal Generator/Calibrator. The IEEE-488 bus is the interface between the central controller and the signal generator/calibrator and HP-IB clock. All items on the bus have the standard IEEE-488 bus interface. Listed below are the devices on the bus, the IEEE-488 interface connector, and the allowable modes of operation on the bus.

IEEE-488 Bus Device	Conn	IEQ Defined Functions			
		Bus Sys Ctrlr	Ctrlr-In-Chg	Talk	Listen
IEQ11 Bus Ctrlr	J1	X	X	X	X
HP59309 HP-IB Clk	A2J2			X	X
HP8565A Calibrator	HP-IB			X	X

The IEQ11 bus controller connects the Qbus to the IEEE-488 Bus. The bus is common to both the primary and secondary systems, and each system has a connected IEQ11. Connector J1 is a 40-pin Bergcon; an interface cable provides the standard IEC 25-pin connector. This connection is described in Section 2.2.6. The bus system controller activates the "Interface Clear" (IFC) (pin 9) and the "Remote Enable" (REN) (pin 17) control signals.

3. CRITICAL TIMING PATHS

Several data processing items in the DSPR system have critical timing paths. These include alert processing, interferometer data processing, and data communications to the Space Surveillance Processing Center.

3.1 Target Detection and Selection Subsystem

Processing in this subsystem is time critical for two reasons. First, antenna data is fed to this subsystem and to the interferometer data collection subsystem simultaneously. Therefore, the target selection process must be completed in the shortest time possible, so that the amount of data lost in the interferometer subsystem is minimal. The primary system double buffers the data in the MAP 4000 and processes data in blocks of 2048 samples. At a 75-kHz sample rate, a buffer is ready for processing every 27.3 ms. Consequently, the array processor must have finished its processing on the previous block within this time. In the secondary system, data is double-buffered in blocks of 8192 samples, which take 109 ms to collect. A half-Doppler and quarter-Doppler detection cycle must be completed within this time. Summarized below are the steps involved in alert data processing and target selection.

The APIO card performs the alert data extraction and transmission in the following steps.

1. Receive data from DD&TC
2. Extract alert data
3. Pass data to the MAP 4000 through the DIO as requested

3.2 System Timing Subsystem

The KWV11 clock is used to obtain precise time for time stamping the observed data. Set to operate at 10 kHz, the KWV11's counter increments every 0.1 ms. This counter is reset by the 1-pulse-per-second received from the HP 5061B Cesium Beam Time Standard. Each pulse generates an interrupt from the KWV11 to the central controller, which is used by a time stamp driver to update the software clock. Whenever interferometer data is time stamped, the hour, minute, and second are read from the software clock. The fractional part of the second is read from the counter register of the KWV11.

Procedure CLOCK is assigned the task of keeping system time. At system startup, the software clock must be set by reading the HP 59309A digital clock. This procedure is given in Appendix E of Volume 1 of this system description[2].

3.3 Data Processing Subsystem

Processing in this subsystem is time critical for the data collection function. The maximum time required for the digital filters to process and output a complete cycle of data for each target is 1.0374 seconds in the primary system. Because each filter operates independently, up to three targets can be processed simultaneously in a 1-second interval. However, the data reduction procedure can only process data from one filter at a time. It is necessary that data reduction on three filter outputs is completed in 1.0374 seconds. As a result, the computational time for the antenna data processing procedure is restricted to 300 ms. The data processing procedure in the central controller performs the antenna data processing. This procedure is described in Section 6 of Volume 1 of this system description[3].

3.4 Interferometer Data Collection Subsystem

All of the processing functions of this subsystem are time critical. Due to the short period of time that a target is in the system, it is vital that data collection commence as soon as possible after target selection. Also, the time stamp is formed after the reset command is given to the digital filter to begin processing. Hence, there will exist some delay between the time that the time stamp is formed and the reset command is interpreted by the digital filter. This time difference should be less than 0.1 ms since the KWV11 is accurate to this figure. Ideally, it should be less than 0.01 ms to minimize the likelihood of the counter register incrementing while it is being read. GET_TIME, the subroutine that time stamps the interferometer data, raises its priority to the highest level to lock out other processes. GET_TIME returns the priority to its normal level after reading the system time and the counter register of the KWV11.

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[2] Carl J. Morris, Carolyn F. Bryant, Marilyn P. Earl, and Tamara A. Myers, *NAVSPASUR Sensor System Digital Signal Processing Receiver, Volume 1—Hardware and Software Overview*, NRL/FR/8154--93-9577, Sept. 1993.

[3] Ibid.

4. HIGH-ALTITUDE SYSTEM

This section describes the hardware differences between the low-altitude and high-altitude receiver stations. The hardware configuration of the high-altitude stations is very similar to that of the low-altitude (normal) stations, but with greater detection capability due to a larger, more sensitive antenna field. This antenna field allows detection of smaller or more distant orbiting objects.

4.1 RF Subsystem

The high-altitude station has 11 antenna arrays and two alert signals, designated as East Alert and West Alert. A spare channel brings the number of receiver channels required to 14. This is the same number required for the low-altitude station, which has 12 antenna arrays, one alert signal, and one spare channel. Consequently, the signal processing within the subsystem is identical between the two stations.

4.2 Target Detection and Selection Subsystem

Because the high-altitude stations have two alert channels, the capacity for twice the alert processing within the same time period is required. This increased capacity is accomplished by using two APIOs and two CSPI MAP 4000 array processors for each system. Figure 4 shows the configuration.

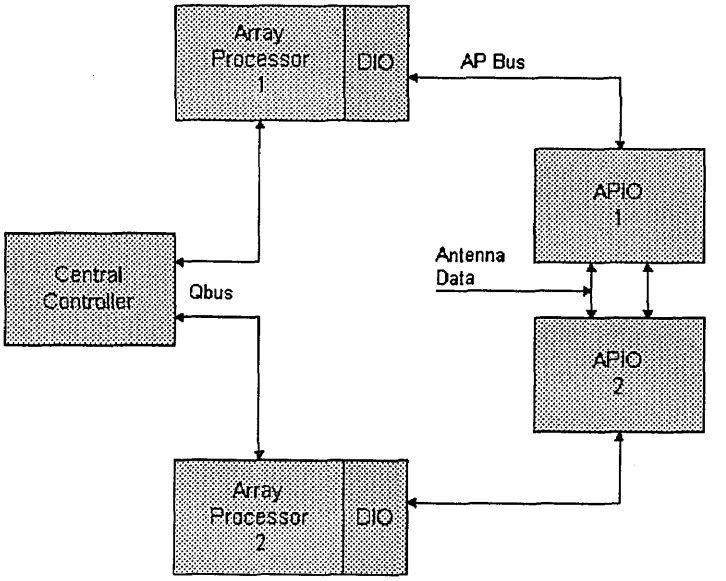
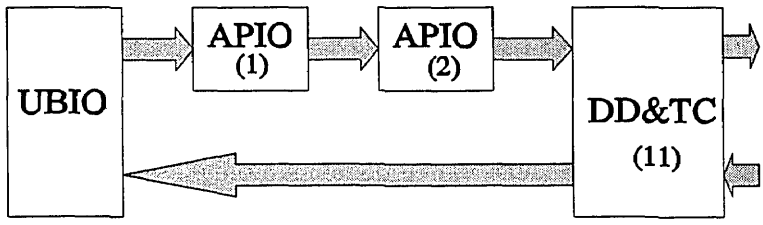


Fig. 4—High-altitude alert interconnections

4.3 Utility Bus Control Subsystem

Due to the additional array processor and APIO in each system, the utility bus is slightly different for the high-altitude station, with two APIO cards in sequence between the UBIO and the DD&TC, as shown in Fig. 5.



Note: Numbers in parentheses are the utility address numbers for the devices

Fig. 5—High-altitude utility bus connections

The connector interface deviations from the low-altitude stations are as follows.

Equipment Connector	Low-altitude Connector	High-altitude Connector
DRV1W J2	DD&TC BG31	APIO West AA31
APIO West AD31	N/A	APIO East AA31
APIO East AD31	N/A	DD&TC BG31
DD&TC AA3	APIO AA31	Misc. CSM BG31
APIO AD31	Misc. CSM BG31	N/A

The pinouts and signal descriptions are given in Sections 2.3 and 2.3.3.

5. ACKNOWLEDGMENTS

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ACRONYMS AND ABBREVIATIONS

A/D	analog-to-digital
APIO	array processor input/output
CSM	command status modules
DD&TC	data distribution and test card
DEC	Digital Equipment Corporation
DF	digital filter
DFIO	digital filter input/output
DFT	discrete Fourier transform
DIO	direct input/output
DSPR	Digital Signal Processing Receiver
HINT	host interface
HP	Hewlett-Packard
IC	integrated circuit
ICC	interprocessor communications (formerly inter-controller communications)
I/O	input/output
kHz	kilohertz
LO	local oscillator
MAP	MAP 4000 Array Processor
MHz	megahertz
ms	milliseconds
NAVSPACECOM	Naval Space Command (formerly Naval Space Surveillance (NAVSPASUR))
NRL	Naval Research Laboratory
OPTEST	operational test
PN	part number
pps	pulse per second
RF	radio frequency
SPADATS	Space Detection and Tracking System
TRGSEL	Target Selection
UB	utility bus
UBIO	utility bus input/output